124471

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 6/14/04 Serial # 10/021,194 Priority Application Date 19981120

Your Name M. Lewis Examiner # ______

AU 2822 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

06-14-04 A...

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: ______

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. ______

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other ______

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 17-19 & 20-25

Problem: See pages 1 & 2
Solution: " " 2 & 3

Please look for the ~~...~~ materials that are disclosed.

Staff Use Only	Type of Search	Vendors
Searcher: Hertzog	Structure (#) ___	STN ✓
Searcher Phone: 2-2663	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, JEF-4B68	Litigation ___	Questel/Orbit ___
Date Searcher Picked Up: 6/17/4	Fulltext ✓	Lexis-Nexis ___
Date Completed: 6/18/4	Patent Family ___	WWW/Internet ___
Searcher Prep/Rev Time: 380	Other ___	Other ___
Online Time: 120		

STIC Search Report
EIC 2800

STIC Database Tracking Number: 124471

TO: Monica Lewis
Location: JEF 5A30
Art Unit : 2822
Friday, June 18, 2004

Case Serial Number: 10/021174

From: Scott Hertzog
Location: EIC 2800
JEF4B68
Phone: 272-2663

Scott.hertzog@uspto.gov

Search Notes

Examiner Lewis,

Attached are edited search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

Also, I discovered that the Kimura reference has a US equiv, it's attached.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Hertzog

```
     FILE 'DPCI' ENTERED AT 07:34:51 ON 18 JUN 2004
L1          2 S (US 6342442 OR US 5391514)/PN
L2            SEL  L1 1- PN.D :      19 TERMS
L3         15 S L2/PN
L4            SEL  L3 1- PN.G :     244 TERMS
L5        214 S L4/PN
L6            SEL  L5 1- PN.D :    2644 TERMS
L7       1976 S L6/PN
L8            SEL  L7 1- PN.G :   26818 TERMS
L9      22224 S L8/PN
L11     23279 S L3 OR L5 OR L7 OR L9
L12         8 S ((LOW? OR REDUC? OR DECREAS? OR LESS?)(A)(BOND? OR
                PROCESS?))(A)TEMPERATURE#
L13       663 S (HIGH?(W)TEMP?)(2A)JOINT# OR REMELT? OR RE(W)MELT?
L14     24806 S MULTILAYER? OR MULTI?(W)LAYER? OR INTERMETALLIC? OR
                INTER(W)METALLIC?
L15     23157 S SOLDER? OR BRAZ? OR BRASING OR BRASED
L16     11274 S BINARY OR TWO(3W)METALS OR BIMETAL? OR BI(W)METAL? OR AU(A)SN OR
                GOLD(A)TIN
L17      1409 S (SOLID(A)LIQUID)(A)(INTER(W)DIFFUSION OR INTERDIFFUSION) OR SLID OR
                TFB OR TRANSFUSION(A)BOND? OR DIFFUSION(A)SOLDER###
L18      3859 S ((L12 OR L13 OR L14 OR L15 OR L16 OR L17)) AND L11
L19           SEL  L18 1- AN :    3859 TERMS

     FILE 'HCAPLUS' ENTERED AT 08:24:26 ON 18 JUN 2004
              S (7439-89-6 OR 7440-02-0 OR 7440-06-4 OR 7440-48-4)/REG#

     FILE 'REGISTRY' ENTERED AT 08:24:27 ON 18 JUN 2004
L20         4 S (7439-89-6 OR 7440-02-0 OR 7440-06-4 OR 7440-48-4)/RN

     FILE 'HCAPLUS' ENTERED AT 08:24:28 ON 18 JUN 2004
L21    769340 S L20
              S (7440-31-5)/REG#

     FILE 'REGISTRY' ENTERED AT 08:24:29 ON 18 JUN 2004
L22         1 S (7440-31-5)/RN

     FILE 'HCAPLUS' ENTERED AT 08:24:29 ON 18 JUN 2004
L23     87268 S L22
              S (7440-57-5)/REG#

     FILE 'REGISTRY' ENTERED AT 08:24:30 ON 18 JUN 2004
L24         1 S (7440-57-5)/RN

     FILE 'HCAPLUS' ENTERED AT 08:24:30 ON 18 JUN 2004
L25    139649 S L24
L26     32339 S L21 AND L22
              S (270252-50-1 OR 270252-51-2)/REG#

     FILE 'REGISTRY' ENTERED AT 08:24:32 ON 18 JUN 2004
L27         2 S (270252-50-1 OR 270252-51-2)/RN

     FILE 'HCAPLUS' ENTERED AT 08:24:32 ON 18 JUN 2004
L28         2 S L27
L29      7270 S L27 OR (L23 AND L25 AND L21)
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    FILE 'DPCI' ENTERED AT 08:39:55 ON 18 JUN 2004
L33             SEL  L18 1- PRN :     5383 TERMS

    FILE 'HCAPLUS' ENTERED AT 08:43:24 ON 18 JUN 2004
L34          2031 S L33
L35            55 S L34 AND L29
L36             0 S L35 NOT P/DT NOT PY>1998
L37            37 S L35 AND ((WO OR US)/AC(P)AD<19981120 OR PD<19981120)
L38          2237 S ((LOW? OR REDUC? OR DECREAS? OR LESS?)(A)(BOND? OR
                    PROCESS?))(A)TEMPERATURE#
L39         13996 S (HIGH?(W)TEMP?)(2A)JOINT# OR REMELT? OR RE(W)MELT?
L40        167751 S MULTILAYER? OR MULTI?(W)LAYER? OR INTERMETALLIC? OR
                    INTER(W)METALLIC?
L41         80862 S SOLDER? OR BRAZ? OR BRASING OR BRASED
L42        171816 S BINARY OR TWO(3W)METALS OR BIMETAL? OR
                  BI(W)METAL? OR AU(A)SN OR GOLD(A)TIN
L43          1578 S (SOLID(A)LIQUID)(A)(INTER(W)DIFFUSION OR INTERDIFFUSION) OR SLID OR
                    TFB OR TRANSFUSION(A)BOND? OR DIFFUSION(A)SOLDER###
L44            32 S L37 AND (L38 OR L39 OR L40 OR L41 OR L42 OR L43)

    FILE 'EUROPATFULL, FRFULL, PATDPAFULL, PCTFULL, RDISCLOSURE, USPATFULL,
    USPAT2' ENTERED AT 09:07:37 ON 18 JUN 2004
L50             QUE L38 AND L39 AND L49
L51           101 S L50

    FILE 'HCAPLUS, EUROPATFULL, PCTFULL, USPATFULL, USPAT2' ENTERED AT 09:33:41 ON 18
L52           131 DUP REM L44 L51 (2 DUPLICATES REMOVED)

    FILE 'EUROPATFULL, FRFULL, PATDPAFULL, PCTFULL, RDISCLOSURE, USPATFULL,
    USPAT2' ENTERED AT 09:44:21 ON 18 JUN 2004
L53            68 S L52 AND ((WO OR US)/AC(S) AD<19981120 OR PD<19981120)
L54            31 S L53 AND (L40 OR L41 OR L42 OR L43)
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File   2:INSPEC 1969-2004/Jun W1
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Jun W2
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Jun W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  25:Weldasearch 19662004/Dec
         (c) 2004 TWI Ltd
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jun W1
         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jun W2
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/May W4
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/Jun B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/Jun W1
         (c) 2004 INIST/CNRS
File 239:Mathsci 1940-2004/Aug
         (c) 2004 American Mathematical Society
File 241:Elec. Power DB 1972-1999Jan
         (c) 1999 Electric Power Research Inst.Inc
File 305:Analytical Abstracts 1980-2004/May W4
         (c) 2004 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2004/May
         (c) 2004 DECHEMA
File 987:TULSA (Petroleum Abs) 1965-2004/Jun W3
         (c)2004 The University of Tulsa

Set     Items   Description
S1       2568   ((LOW OR LOWER OR LOWEST OR REDUC? OR DECREAS? OR LESS?)(N-
             )(BOND? OR PROCESS?))(N)TEMPERATURE#
S2      13496   ((HIGH OR HIGHER OR HIGHEST OR GREATER)(W)(TEMP OR TEMPERA-
             TURE#))(2N)JOINT# OR REMELT? OR RE(W)MELT?
S3     443739   MULTILAYER? OR (MULTIPLE# OR MULTITUDE# OR MULTI)(W)LA-
             YER? OR INTERMETALLIC? OR INTER(W)METALLIC?
S4     281853   SOLDER? OR BRAZ? OR BRASING OR BRASED
S5     632619   BINARY OR TWO(3W)METALS OR BIMETAL? OR BI(W)(METALLIC OR M-
             ETAL#) OR AU(N)SN
S6          4   S1 AND S2 AND (S3 OR S5) AND S4
S7          4   RD (unique items)
S8         92   S2 AND (S3 OR S5) AND S4
S9         88   S8 NOT S7
S10        54   RD (unique items)
S11        22   S10 NOT PY>1998
```

DERWENT-ACC-NO: 1996-079768

DERWENT-WEEK: 200324

TITLE: Material for e.g. soldering semiconductor laser device to pedestal - comprises alloy of gold@, tin@ and nickel@ and formed by heating layered structure of gold@-tin@ alloy and nickel@

INVENTOR: ABE, K; ATSUMI, K ; KIMURA, Y ; MATSUSHITA, N ; MIZUTANI, M ; TOYAMA, T

PATENT-ASSIGNEE: NIPPONDENSO CO LTD[NPDE]

PRIORITY-DATA: 1995JP-0140175 (June 7, 1995) , 1994JP-0179935 (August 1, 1994) , 1994JP-0264719 (October 28, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
CA 2155091 C	March 25, 2003	E	000	B23K 035/26
GB 2291886 A	February 7, 1996	N/A	044	C22C 005/02
CA 2155091 A	February 2, 1996	N/A	000	B23K 035/26
JP 08181392 A	July 12, 1996	N/A	010	H01S 003/18
GB 2291886 B	February 25, 1998	N/A	000	C22C 005/02
US 5794839 A	August 18, 1998	N/A	000	H01L 021/58

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
CA 2155091C	N/A	1995CA-2155091	July 31, 1995
GB 2291886A	N/A	1995GB-0015696	July 31, 1995
CA 2155091A	N/A	1995CA-2155091	July 31, 1995
JP 08181392A	N/A	1995JP-0140175	June 7, 1995
GB 2291886B	N/A	1995GB-0015696	July 31, 1995
US 5794839A	N/A	1995US-0509234	July 31, 1995

INT-CL (IPC): B23K035/26, C22C005/02 , H01L021/58 , H01L023/40 , H01L023/488 , H01S003/18

RELATED-ACC-NO: 1996-479441

ABSTRACTED-PUB-NO: GB 2291886A

BASIC-ABSTRACT:

Material for bonding a device electrode to a pedestal is an Au-based alloy contg. Sn and Ni, the Ni content being 1.3-10 (pref. 2-5) wt%. The alloy is pref. formed by heating a layered structure of an Au-Sn alloy layer and an Ni layer. An electric device is mounted on a pedestal by: forming an electrode layer on the element; forming an Ni layer followed by an Sn-contg. solder layer directly on the electrode layer; and heating to cause layer diffusion to form an ohmic contact bond between element and pedestal. The Sn-contg. solder layer is pref. a (PVD) Au-Sn alloy layer.

USE - In soldering e.g. a semiconductor laser device to a pedestal (claimed).

ADVANTAGE - Mutual diffusion of the Ni and solder layers provides high bonding strength and improved solder wettability, without need for a formed pellet of eutectic solder.

ABSTRACTED-PUB-NO: GB 2291886B

EQUIVALENT-ABSTRACTS:

Material for bonding a device electrode to a pedestal is an Au-based alloy contg. Sn and Ni, the Ni content being 1.3-10 (pref. 2-5) wt%. The alloy is pref. formed by heating a layered structure of an Au-Sn alloy layer and an Ni layer. An electric device is mounted on a pedestal by: forming an electrode layer on the element; forming an Ni layer followed by an Sn-contg. solder layer directly on the electrode layer; and heating to cause layer diffusion to form an ohmic contact bond between element and pedestal. The Sn-contg. solder layer is pref. a (PVD) Au-Sn alloy layer.

USE - In soldering e.g. a semiconductor laser device to a pedestal (claimed).

ADVANTAGE - Mutual diffusion of the Ni and solder layers provides high bonding
strength and improved solder wettability, without need for a formed pellet of
eutectic solder.

US 5794839A

Material for bonding a device electrode to a pedestal is an Au-based alloy
contg. Sn and Ni, the Ni content being 1.3-10 (pref. 2-5) wt%. The alloy is
pref. formed by heating a layered structure of an Au-Sn alloy layer and an Ni
layer. An electric device is mounted on a pedestal by: forming an electrode
layer on the element; forming an Ni layer followed by an Sn-contg. solder layer
directly on the electrode layer; and heating to cause layer diffusion to form
an ohmic contact bond between element and pedestal. The Sn-contg. solder layer
is pref. a (PVD) Au-Sn alloy layer.

USE - In soldering e.g. a semiconductor laser device to a pedestal (claimed).

ADVANTAGE - Mutual diffusion of the Ni and solder layers provides high bonding
strength and improved solder wettability, without need for a formed pellet of
eutectic solder.

CHOSEN-DRAWING: Dwg.1/9 Dwg.1

TITLE-TERMS: MATERIAL SOLDER SEMICONDUCTOR LASER DEVICE PEDESTAL COMPRISE ALLOY
GOLD@ TIN@ NICKEL@ FORMING HEAT LAYER STRUCTURE GOLD@ TIN@ ALLOY
NICKEL@

DERWENT-CLASS: L03 M26 P55 U11 U12 V08

CPI-CODES: L04-E03B; L04-F02; M23-A01; M23-A04; M26-B01; M26-B01N; M26-B01T;

EPI-CODES: U11-C05E1; U11-C05F6; U11-D03B2; U12-A01B2; V08-A04A;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1996-026420
Non-CPI Secondary Accession Numbers: N1996-066351

+=

7/9/3 (Item 2 from file: 8)
DIALOG(R)File 8:**Ei Compendex**(R)

05089251 E.I. No: EIP98084333022
Title: **High temperature joints** manufactured at low temperature
Author: So, William W.; Lee, Chin C.
Corporate Source: Univ of California, Irvine, CA, USA
Conference Title: Proceedings of the 1998 48th Electronic Components & Technology Conference
Conference Location: Seattle, WA, USA
Conference Date: 19980525-19980528
Sponsor: IEEE
E.I. Conference No.: 48782
Source: Proceedings - Electronic Components and Technology Conference 1998. IEEE, Piscataway, NJ, USA,98CB36206. p 284-291
Publication Year: 1998
CODEN: PECCA7 ISSN: 0569-5503

Journal Announcement: 9810W1
Abstract: A fluxless bonding process using either indium-silver or tin-copper **multilayer** composite to produce **high temperature joints** at relatively low temperature has been developed. The process temperatures for indium-silver and tin-copper system are 210 degree C and 280 degree C, respectively. Joints, which are almost void-free, with melting temperatures of 210 degree C and 415 degree C, respectively, are made. After further annealing at 150 degree C for In-Ag and 280 degree C for Sn-Cu, the **re-melting** temperature of the joints increases to above 700 degree C. The technique, thus, provides a quantum jump to the post-processing temperature of component fabrication. In either process, the joints are examined using a scanning acoustic microscope to confirm the bonding quality. The joint cross-sections are studied using SEM and EDX to find the microstructure and composition. Upon deposition, In interacts with Ag to become In-AgIn//2 composite, and Sn interacts with Cu to become Sn-Cu//6Sn//5 composite. The **intermetallic** compounds AgIn//2 and Cu//6Sn//5 prevent the In and Sn layers from oxidation in atmosphere. Thus no flux is needed. Besides the fluxless feature, the **low process temperature** would significantly reduce the stresses developed due to thermal expansion mismatch comparing to the otherwise high temperature processes with temperature exceeding the melting temperature. The **multilayer** bonding method also facilitates precise control of the alloy composition and the joint thickness. The new technique should find applications in the emergent high temperature electronic devices. (Author abstract) 22 Refs.
Descriptors: **Soldered joints; High temperature** operations; Copper alloys; Indium alloys; Annealing; Scanning electron microscopy; X ray analysis; Thermal expansion; **Intermetallics;** Oxidation
Identifiers: **High temperature joints;** Scanning acoustic microscope
Classification Codes:
538.1.1 (Soldering)
538.1 (Metal Bonding); 931.2 (Physical Properties of Gases, Liquids & Solids); 544.2 (Copper Alloys); 549.3 (Others, including Bismuth, Boron,

Cadmium, Cobalt, Mercury, Niobium, Selenium, Silicon, Tellurium & Zirconium); 537.1 (Heat Treatment Processes); 741.1 (Light/Optics)
538 (Welding & Bonding); 931 (Applied Physics); 544 (Copper & Alloys); 549 (Nonferrous Metals & Alloys); 537 (Heat Treatment); 741 (Optics & Optical Devices)
53 (METALLURGICAL ENGINEERING); 93 (ENGINEERING PHYSICS); 54 (METAL GROUPS); 74 (OPTICAL TECHNOLOGY)

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7/9/4 (Item 1 from file: 35)
DIALOG(R)File 35:**Dissertation Abs Online**

01504372 ORDER NO: AAD96-30178
FLUXLESS OXIDATION-FREE BONDING TECHNOLOGY USING COPPER AND SILVER-BASED **MULTILAYER** COMPOSITES (TIN, INDIUM)
Author: CHEN, YI-CHIA
Degree: PH.D.
Year: 1996
Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, IRVINE (0030)
Chair: CHIN C. LEE
Source: VOLUME 57/05-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3384. 133 PAGES
Descriptors: ENGINEERING, METALLURGY ; ENGINEERING, MATERIALS SCIENCE
Descriptor Codes: 0743; 0794

A fluxless oxidation-free bonding technology has been developed using **multilayer** composite **solders** based on Cu-Sn, Cu-In, Ag-Sn, and Ag-In systems. This technology eliminates the use of flux and scrubbing motion while still produces high quality joints. This is achieved by high vacuum direct deposition of the **multilayer** composites on the objects to be joined. The oxidation mechanism in the environment of low oxygen partial pressure is modeled and studied. The results reveal that high vacuum deposition does suppress the oxide growth. The in situ formation of stable **intermetallic** compounds on the outer surface of the composites protects the inner layers from oxidation. GaAs and silicon dice have been successfully bonded on alumina, glass, or silicon substrates. The bonding is achieved by means of solid-liquid interdiffusion (SLID) and in situ compound formation. Nearly void-free joints are fabricated as confirmed by a scanning acoustic microscope (SAM) with a spatial resolution of 20 μm. A scanning electron microscope (SEM) and energy dispersive X-ray (EDX) spectrometer are employed to study the microstructure, **intermetallic** compound formation, grain distribution, and composition of the joints. In addition to the fluxless and oxidation-free features, this technology can produce **high temperature joints** at a relatively low temperature, thus reducing the stress induced by thermal expansion mismatch among the parts. The **remelting** temperature of the joints can be designed by choosing proper composite composition. At a **low bonding temperature** ($\sim$250°C), liquid-solid interdiffusion takes place first, followed by a solid-state diffusion process either in the same bonding process or a post-bonding annealing step. The resulting joint can withstand temperature much higher than the processing temperature, up to 700°C. Consequently, it gives a quantum jump to the post processing temperature. The lower and **lower processing temperature** in conventional

soldering hierarchy is thus reversed. Furthermore, by controlling the compositions, the ratio between different phases in the joints can be adjusted. Therefore, the mechanical properties of the joints such as ductility, yield strength, and hardness can also be controlled. This technology is valuable for various applications where parts are required to join together reliably with precise thickness and composition control without the use of flux.

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11/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

6011953 INSPEC Abstract Number: B9810-2240-005
Title: A low temperature interconnection method for electronics assembly
Author(s): Kulojarvi, K.; Kivilahti, J.K.
Journal: IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A Conference Title: IEEE Trans. Compon. Packag. Manuf. Technol. A (USA) vol.21, no.2 p.288-91
Publisher: IEEE,
Publication Date: June 1998 Country of Publication: USA
CODEN: IMTAEZ ISSN: 1070-9886
SICI: 1070-9886(199806)21:2L.288:TIME;1-C
Abstract: In this communication, a transfusion bonding (TFB) technique of electronic components is briefly explained and illustrated in the context of FC-on-flex, FC-on-FR4, and flex-on-rigid board assemblies utilizing either adhesive or underfiller. The TFB technique with well-controlled local oxide-free liquid transfusion is not based on **intermetallic** formation as conventional **soldering** but on the generation of ductile Sn-based solid solution joints. The composition of the joints are controlled by the relative thicknesses of Sn-based undercoating and Bi overcoating which are deposited on conductors either chemically or electrochemically. The technique is 100% fluxless and is especially suitable for joining temperature-sensitive flexible substrate materials, because the bonding temperatures are well below the melting points of the conventional Pb-containing **solders** . The TFB technique differs from conventional **soldering** also in that the **remelting** temperatures are clearly higher than the bonding temperatures. By combining TFB technique with adhesive joining it is possible to increase the mechanical integrity of the assemblies and to protect the assemblies during operational life. Different aging and cycling tests showed that the TF-bonded microjoints to flexible and rigid substrates are reliable and allow the usage of low cost flexible circuits. (10 Refs)
Subfile: B
Descriptors: adhesion; assembling; flip-chip devices; joining processes
Identifiers: low temperature interconnection; electronics assembly; transfusion bonding; FC-on-FR4; flex-on-rigid board; FC-on-flex; adhesive; underfiller; ductile solid solution; Bi overcoating; Sn-based undercoating; rigid substrate; chemical deposition; electrochemical deposition; flexible substrate; mechanical integrity; aging; cycling; microjoint
Class Codes: B2240 (Microassembly techniques)

+=

11/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:**INSPEC**

5442467 INSPEC Abstract Number: A9702-6865-003, B9701-0550-003
Title: Indium-copper **multilayer** composites for fluxless oxidation-free bonding
Author(s): Chen Yichia; Lee, C.C.
Journal: Thin Solid Films vol.283, no.1-2 p.243-6

Publisher: Elsevier,
Publication Date: 1 Sept. 1996 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
Abstract: A 200 degrees C fluxless process is developed to produce In-Cu joints. The fluxless feature is achieved by preventing indium oxidation during composite fabrication and the subsequent bonding process. Indium and copper are deposited on an object in high vacuum to inhibit indium oxidation. Copper interacts with indium to form a CuIn **intermetallic** that further protects the inner indium from oxidation. For the specific design of this study, the resulting joints consist of CuIn **intermetallic** grains surrounded by pure indium as revealed by scanning electron microscopy with energy dispersive X-ray analysis. Scanning acoustic microscope examination indicates that the joints are nearly void free. This technology enables versatile control of alloy composition, thus leading to several **remelting** temperatures and various physical properties. The CuIn compound was clearly identified in this study even though it was not shown in two published Cu-In phase diagrams. (12 Refs)
Subfile: A B
Descriptors: acoustic microscopy; adhesion; chemical interdiffusion; copper; indium; metallic superlattices; metallic thin films; oxidation; phase diagrams; scanning electron microscopy; **soldering**; solid solutions; vacuum deposited coatings; voids (solid); X-ray chemical analysis
Identifiers: fluxless oxidation free bonding; **multilayer** composites ; high vacuum deposition; **intermetallic** grains; scanning electron microscopy; energy dispersive X ray analysis; scanning acoustic microscopy; void free joints; phase diagrams; 200 C; In-Cu
Class Codes: A6865 (Layer structures, intercalation compounds and superlattices: growth, structure and nonelectronic properties); A8160B (Surface treatment and degradation of metals and alloys); A8280D (Electromagnetic radiation spectrometry (chemical analysis)); A6480G (Microstructure); A6170Q (Inclusions and voids); A6630N (Chemical interdiffusion in solids); B0550 (Composite materials (engineering materials science)); B0530 (Metals and alloys (engineering materials science)); B0170G (General fabrication techniques)
Chemical Indexing:
In-Cu int - Cu int - In int - Cu el - In el (Elements - 1,1,2)
Numerical Indexing: temperature 4.73E+02 K

+=

11/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:**INSPEC**

5249451 INSPEC Abstract Number: B9606-2210D-015
Title: Indium-copper **multilayer** composite **solder** for fluxless bonding
Author(s): Lee, C.C.; Yi-Chia Chen
Conference Title: Electronic Packaging Materials Science VIII. Symposium p.225-30
Editor(s): Sundahl, R.C.; Tu, K.-T.; Jackson, K.A.; Borgesen, P.
Publisher: Mater Res. Soc, Pittsburgh, PA, USA
Publication Date: 1995 Country of Publication: USA xi+284 pp.

Material Identity Number: XX96-00317
Conference Title: Electronic Packaging Materials Science VIII. Symposium
Conference Date: 17-20 April 1995 Conference Location: San Francisco, CA, USA
Abstract: A 200 degrees C fluxless process is developed to produce In-Cu joints. The fluxless feature is achieved by the prevention of indium oxidation during the **solder** fabrication and the bonding process. Indium and copper are deposited on an object in high vacuum to inhibit indium oxidation. Copper interacts with indium to form a CuIn compound that further protects the inner indium from oxidation. For a specific design, the resulting joints consist of mainly CuIn **intermetallic** grains surrounded by a small amount of pure indium as revealed by SEM with EDX. Scanning acoustic microscopy indicates that the joints are nearly void-free. This technology enables versatile control of the alloy composition, thus leading to several **remelting** temperatures and various physical properties. (8 Refs)
Subfile: B
Descriptors: acoustic microscopy; assembling; copper alloys; indium alloys; integrated circuit packaging; oxidation; printed circuit manufacture; scanning electron microscopy; **soldering**; vacuum deposition; voids (solid); X-ray chemical analysis
Identifiers: indium-copper **multilayer** composite **solder;** fluxless bonding; fluxless process; In-Cu joints; indium oxidation prevention; **solder** fabrication; bonding process; indium deposition; copper deposition; high vacuum deposition; CuIn compound; CuIn **intermetallic** grains; SEM; EDX; scanning acoustic microscopy; void-free joints; alloy composition control; **remelting** temperatures; physical properties; 200 C; InCu
Class Codes: B2210D (Printed circuit manufacture); B0170G (General fabrication techniques); B0170J (Product packaging); B0170E (Production facilities and engineering); B0520F (Vapour deposition)
Chemical Indexing:
InCu int - Cu int - In int - InCu bin - Cu bin - In bin (Elements - 2)
Numerical Indexing: temperature 4.73E+02 K

+=
11/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:**INSPEC**

5064169 INSPEC Abstract Number: B9511-2240-004
Title: **High temperature** Cu-Sn **joints** manufactured by a 250 degrees C fluxless bonding process
Author(s): Yi-Chia Chen; Lee, S.J.; Lee, C.C.
Conference Title: Proceedings. 1995 IEEE Multi-Chip Module Conference (Cat. No.95CH35726) p.206-11
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1994 Country of Publication: USA xi+233 pp.
ISBN: 0 8186 6970 5
U.S. Copyright Clearance Center Code: 0 8186 6970 5/94/$04.00
Conference Title: Proceedings of 1995 IEEE Multi-Chip Module Conference (MCMC-95)
Conference Sponsor: IEEE Circuits & Syst. Soc; IEEE Comput. Soc..; IEEE Components, Packaging, & Manuf. Technol. Soc.; IEEE Electron. Devices Soc

Conference Date: 31 Jan.-2 Feb. 1995 Conference Location: Santa Cruz, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: A 250 degrees C bonding process is developed to manufacture Cu-Sn joints that can withstand up to 415 degrees C. This is made possible by solid-liquid interdiffusion in the mixture of Cu, Sn, and Sn liquid that contacts with Cu coated on a substrate. The mixture is produced by heating the Sn-Cu **multilayer** composite that is deposited on semiconductor in high vacuum to inhibit tin oxidation. Upon deposition, Cu interacts with Sn to become Sn-Cu/sub 6/Sn/sub 5/ composite where Cu/sub 6/Sn/sub 5/, prevents the Sn layer from oxidation in atmosphere. Thus no flux is needed. This is a fluxless, lead-free, low cost, low temperature process that provides **high temperature joints.** (11 Refs)
Subfile: B
Descriptors: copper alloys; microassembling; multichip modules; **soldering**; surface mount technology; tin alloys
Identifiers: **high temperature** Cu-Sn **joints**; fluxless bonding process; solid-liquid interdiffusion; Sn-Cu **multilayer** composite; semiconductor; oxidation prevention; lead-free low cost process; low temperature process; 250 C; 415 C; Cu-Sn; Sn-Cu/sub 6/Sn/sub 5
Class Codes: B2240 (Microassembly techniques); B2250 (Multichip modules); B0170G (General fabrication techniques)
Chemical Indexing:
CuSn bin - Cu bin - Sn bin (Elements - 2)
SnCu6Sn5 ss - Cu6 ss - Sn5 ss - Cu ss - Sn ss (Elements - 2)
Numerical Indexing: temperature 5.23E+02 K; temperature 6.88E+02 K

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11/9/5 (Item 1 from file: 8)
DIALOG(R)File 8:**Ei Compendex**(R)

04460760 E.I. No: EIP96083261869
Title: Fabricating high-performance joints by solid-state diffusion bonding- a theoretical and experimental approach
Author: Tillmann, W.; Lugscheider, E.
Corporate Source: Hilti AG, Schaan, Ger
Source: International Journal for the Joining of Materials v 8 n 2 Jun 1996. p 56-61
Publication Year: 1996
CODEN: IJJMEY ISSN: 0905-6866
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 9610W1
Abstract: In comparison to conventional high-temperature **brazing** the diffusion bonding processes incorporates several interesting features, which makes this technology a challenging alternative for the fabrication of high-performance joints. During the diffusion joining process an interlayer foil is placed in between the parent metals and is heated up to the eutectic temperature. Owing to solid state diffusion there is a solution of the base metal in the interlayer and a temporary liquid phase is formed. The combination Ni-Hf-Ni is used to study the metallurgical

effects. Apart from utilizing the diffusion bonding process to the joining of metallic base materials it is also possible to fabricate heat-resistant ceramic joints by employing solid-state diffusion bonding techniques. By using suitable interlayer combinations consisting of a reactive metal and an eutectic forming element it is possible to fabricate heat resistant joints that obtain a **remelting**-temperature higher than the actual **brazing** temperature. Within the scope of the paper preliminary results on the diffusion bonding of silicon-nitride employing a reactive interlayer system are presented and analysed. (Author abstract) 5 Refs.

Descriptors: Bonding; Joints (structural components); Fabrication; Diffusion in solids; Metallurgy; **Brazing**; Temperature; **Multilayers**; Heat resistance; Joining

Identifiers: High performance joints; Solid state diffusion bonding; Transient liquid phase bonding; Diffusion joining; Eutectic forming element

Classification Codes:

538.1.1 (Soldering)

802.3 (Chemical Operations); 408.2 (Structural Members & Shapes); 931.2 (Physical Properties of Gases, Liquids & Solids); 531.1 (Metallurgy); 538.1 (Metal Bonding); 641.1 (Thermodynamics)

802 (Chemical Apparatus & Plants); 408 (Structural Design); 931 (Applied Physics); 531 (Metallurgy & Metallography); 538 (Welding & Bonding); 641 (Heat & Thermodynamics)

80 (CHEMICAL ENGINEERING); 93 (ENGINEERING PHYSICS); 53 (METALLURGICAL ENGINEERING); 64 (HEAT & THERMODYNAMICS)

+=

11/9/6 (Item 2 from file: 8)

DIALOG(R)File 8:**Ei Compendex**(R)

03974825 E.I. No: EIP94112405148

Title: Diffusion **soldering** for electronics manufacturing

Author: Humpston, G.; Jacobson, D.M.; Sangha, S.P.S.

Corporate Source: GEC-Marconi Ltd, Borehamwood, Engl

Source: Endeavour v 18 n 2 1994. p 55-60

Publication Year: 1994

CODEN: ENDEAS ISSN: 0160-9327

Journal Announcement: 9412W4

Abstract: Diffusion **soldering** is a joining method that combines features of conventional **soldering** and diffusion bonding processes. The process relies on reaction between a thin layer of molten **solder** and metal on the components to form one or more **intermetallic** phases that are solid at the joining temperature. The joint will not **remelt** thereafter unless it is heated to a higher temperature at which one of the **intermetallic** phases melts. This article reviews the principles of the process and its application to electronics component manufacturing. (Author abstract) 14 Refs.

Descriptors: **Soldering**; Diffusion; **Soldering** alloys; Metals; Molten materials; Electronic equipment manufacture; **Soldered** joints; Heating; Surfaces

Identifiers: Diffusion **soldering**; **Intermetallic** phases; Joining temperature; Thermomechanical integrity

Classification Codes:

538.1.1 (Soldering)

538.1 (Metal Bonding); 641.3 (Mass Transfer); 801.1 (Chemistry,

General); 715.2 (Industrial Electronic Equipment); 641.2 (Heat Transfer)
538 (Welding & Bonding); 641 (Heat & Thermodynamics); 801 (Chemical Analysis & Physical Chemistry); 715 (General Electronic Equipment)
53 (METALLURGICAL ENGINEERING); 64 (HEAT & THERMODYNAMICS); 80 (CHEMICAL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS)

+=

11/9/9 (Item 2 from file: 25)
DIALOG(R)File 25:**Weldasearch**

00200102 179643
Fluxless oxidation-free bonding technology using copper and silver-based **multilayer** composites.
CHEN Y C
UNIVERSITY OF CALIFORNIA, IRVINE
Thesis (Ph.D). University of California, Irvine, CA 92717, USA; 1996.
133pp.
PUBLICATION DATE: 19960000 DOCUMENT TYPE: Thesis
LANGUAGE: English RECORD TYPE: Abstract

A fluxless oxidation-free bonding technology was developed using **multilayer** composite **solders** based on Cu-Sn, Cu-In, Ag-Sn, and Ag-In systems. This technology eliminates the use of flux and scrubbing motion while still producing high quality joints. This is achieved by high vacuum direct deposition of the **multilayer** composites on the objects to be joined under low oxygen partial pressure. GaAs and silicon dice were bonded on alumina, glass, or silicon substrates. The bonding is achieved by means of solid-liquid interdiffusion (SLID) and in situ compound formation. Microstructure, **intermetallic** compound formation, grain distribution, and composition of the joints are reported. The use of the technology to produce **high temperature joints** at a relatively low temperature is described.
[See also Weldasearch 177107, 174375, 175443, 167443 and 166672]

FILE SEGMENT: Technical
TREATMENT CODE: Experimental
COUNTRY: USA
TWI AVAILABILITY: No
CROSS REFERENCES: 177107; 174375; 175443; 167443; 166672
DESCRIPTORS: THESES; **SOLDERS**; FILLER MATERIALS; COPPER; TIN; INDIUM; SILVER; SILICON; ALUMINA; CERAMICS; OXIDES; GLASS; DIFFUSION **SOLDERING**; DIFFUSION BONDING; **SOLDERING**; MICROSTRUCTURE; **INTERMETALLICS**; SCOPE; GRAIN SIZE; HIGH TEMPERATURE; TEMPERATURE; PROCESS VARIANTS; OXIDATION; CHEMICAL REACTIONS; MICROJOINING
SECTION HEADING: **SOLDERING**; MICROJOINING

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11/9/13 (Item 6 from file: 25)
DIALOG(R)File 25:**Weldasearch**

00171057 150598
Diffusion **soldering**.
JACOBSON D M; HUMPSTON G

Soldering and Surface Mount Technology, no.10. **Feb.1992**. pp.27-32. 8 fig., 1 tab., 12 ref.
SOLDERING AND SURFACE MOUNT TECHNOLOGY
PUBLICATION DATE: 19920000 DOCUMENT TYPE: Journal
LANGUAGE: English RECORD TYPE: Abstract

Features of diffusion **soldering** (with special reference to Cu-Sn, Ag-Sn, Ag-In, and Ag-In-Sn systems), and benefits of applying the process to the fabrication of electronics assemblies are explained. Topics include: diffusion **soldering** principles, reaction kinetics, and mechanisms of bond formation (production of **intermetallic** compounds); suitability for alloys of Al, Co, Cu, Ni, Ag, Ti, and steels; advantages (lower pressure required than diffusion welding or **brazing**, good joint filling, crisp edges); and properties of the different alloy systems (**remelt** temperature, joint properties, bond strength). Other applications include components with different coefficients of thermal expansion e.g. heavy duty power devices and production of reliable hermetic seals.
Similar paper in: High Technology Joining. Proceedings, 6th BABS International Conference, Stratford-upon-Avon, 3-5 Sept.1991. Publ: Wantage, OX12 9BJ, UK; Margaret Swadling Conference Services for British Association for **Brazing** and **Soldering**; 1991. Paper 4. 15pp; Weldasearch 149000]

FILE SEGMENT: Technical
TWI AVAILABILITY: Yes
CROSS REFERENCES: 149000
DESCRIPTORS: ALUMINIUM; **BRAZING**; CHEMICAL REACTIONS; COMPARISONS; COMPONENTS; COPPER; DIFFUSION; DIFFUSION BONDING; DIFFUSION **BRAZING** ; DIFFUSION WELDING; ELECTRONIC DEVICES; INDIUM; **INTERMETALLICS**; LIGHT METALS; MECHANICAL PROPERTIES; MECHANISMS; MICROJOINING; NICKEL; PHYSICAL PROPERTIES; PRESSURE; REFERENCE LISTS; SCOPE; SILVER; **SOLDERED** JOINTS; **SOLDERING**; STRENGTH; TEMPERATURE; THERMAL PROPERTIES; TIN; TITANIUM; UTILISATION

+=
11/9/14 (Item 7 from file: 25)
DIALOG(R)File 25:**Weldasearch**

00170373 149914
Au-Sn transient liquid bonding in high performance laminates.
INTERNATIONAL BUSINESS MACHINES CORP
European Patent Application 461 378 A2. Filed: 30 Apr.1991 (USA 536145, 11 June 1990). Publ: 18 Dec.1991. 10 fig., 12 claims.
PATENT (NUMBER,DATE): **US 5280414** A2 **19911218**
APPLICATION DATE: 19910430
PRIORITY (NO, DATE): **US 536145-1990 19900611**

A method of making electrical interconnections between laminated layers of composite material in printed circuit (PCB) manufacture is claimed. Two elements are selected which will form a eutectic at a low temperature and will solidify to form an alloy which will only **remelt** at a second temperature higher than any required by any subsequent lamination. A transient liquid bonding technique is used where one metal (e.g. gold) is

deposited on a land and another (e.g. tin) is deposited on the corresponding land with which it is to be connected. A **Au-Sn** 20 wt.% eutectic is formed at the low temperature. Once solidified the alloy remains solid throughout subsequent laminations and a composite, **multilayered** high performance PCB is produced.

FILE SEGMENT: Technical
TWI AVAILABILITY: No
DESCRIPTORS: **BRAZING**; DIFFUSION BONDING; DIFFUSION **BRAZING**; ELECTRIC CIRCUITS; EUROPE; EUTECTICS; GOLD; LAMINATES; PATENTS; PLASTICS; PRINTED CIRCUITS; TIN; USA

☐ **L44 ANSWER 1 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:102249 HCAPLUS Full Text

Title

Method for forming reflowed solder ball with low melting point metal cap

Author/Inventor

Dalal, Hormazdyar Minocher; Bitaillou, Alexis; Fallon, Kenneth Michael; Gaudenzi, Gene Joseph; Herman, Kenneth Robert; Pierre, Frederic; Robert, Georges

Patent Assignee/Corporate Source

International Business Machines Corporation, USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6344234	B1	20020205	US 1995-476475	19950607 <--
			US 1995-476475	19950607

Abstract

A method and structure for a ***solder*** interconnection, using ***solder*** balls for making a low temperature chip attachment directly to any of the higher levels of packaging substrate is disclosed. After a ***solder*** ball has been formed using standard methods it is reflowed to give the ***solder*** ball a smooth surface. A layer of low m.p. metal, such as, Bi, In or Sn, preferably, pure Sn, is deposited on the top of the ***solder*** balls. This structure results in localizing of the eutectic alloy, formed upon subsequent low temperature joining cycle, to the top of the high melting ***solder*** ball even after multiple low temperature reflow cycles. This method does not need tinning of the substrate to which the chip is to be joined, which makes this method economical. It has also been noticed that whenever temperature is raised slightly above the eutectic temperature, the structure always forms a liquid fillet around the joint with Cu wires. This liquid fillet formation results in substantial thermal fatigue life improvement for reduced stress at interface; and secondly, provides an easy means to remove chip for the purpose of chip burn-in, replacement or field repairs.

Concept or Classification

76-2 (Electric Phenomena)

Supplementary Terms

reflow ***solder*** ball interconnection

Controlled or Index Terms

Coating process
(electroless; method for forming reflowed ***solder*** ball with low m.p. metal cap)
Capacitors
Electrodeposition
Electronic packages
Electronic packaging process
Etching
Integrated circuits
Interconnections, electric
Joining
Resistors
Vapor deposition process
(method for forming reflowed ***solder*** ball with low m.p. metal cap)
Polyimides, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(method for forming reflowed ***solder*** ball with low m.p. metal

cap)
Soldering
(reflow; method for forming reflowed ***solder*** ball with low m.p. metal cap)
Ceramics
(substrates; method for forming reflowed ***solder*** ball with low m.p. metal cap)
7440-57-5 , Gold, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(contact material, ***solder*** ball material; method for forming reflowed ***solder*** ball with low m.p. metal cap)
7439-89-6 , Iron, uses ***7440-02-0*** , Nickel, uses
7440-47-3, Chromium, uses ***7440-48-4*** , Cobalt, uses 7440-50-8, Copper, uses 12642-02-3
RL: TEM (Technical or engineered material use); USES (Uses)
(contact material; method for forming reflowed ***solder*** ball with low m.p. metal cap)
7439-92-1, Lead, uses 7440-22-4, Silver, uses ***7440-31-5*** , Tin, uses 7440-69-9, Bismuth, uses 7440-74-6, Indium, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(***solder*** ball material; method for forming reflowed ***solder*** ball with low m.p. metal cap)
11110-87-5 80954-92-3
RL: TEM (Technical or engineered material use); USES (Uses)
(***solder*** ; method for forming reflowed ***solder*** ball with low m.p. metal cap)

National Patent Classification
427096000

International Patent Classification
ICM B05D005-12

☐ L44 ANSWER 2 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
2001:721475 HCAPLUS Full Text

Title
Structure, materials, and applications of ball grid array interconnections

Author/Inventor
Call, Anson J.; Delaurentis, Stephen Anthony; Farooq, Shaji; Kang, Sung Kwon; Purushothaman, Sampath; Stalter, Kathleen Ann

Patent Assignee/Corporate Source
International Business Machines Corporation, USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6297559	B1	20011002	US 1998-107998	19980630 <--
			US 1997-52175P P	19970710

Abstract
A new interconnection scheme of a ball grid array (BGA) module is disclosed where a ***solder*** ball is connected to the BGA module using an elec. conducting adhesive The elec. conducting adhesive can be a mixture comprising a polymer resin, no-clean ***solder*** flux, a plurality of elec. conducting particles with an elec. conducting fusible coating and others. The ***solder*** balls in a BGA module can also be connected to a printed circuit board using another elec. conductive adhesive which can be joined at a lower temperature than the 1st joining to the BGA module. Addnl., an elec. conducting adhesive can be formed into elec.

conducting adhesive bumps which interconnect an integrated circuit device to the BGA module.

Concept or Classification

76-3 (Electric Phenomena)

Supplementary Terms

ball grid array interconnection

Controlled or Index Terms

Integrated circuits
Interconnections (electric)
Joining
Semiconductor devices
Solders
(structure, materials, and applications of ball grid array interconnections)
7429-90-5, Aluminum, processes 7439-92-1, Lead, processes 7440-05-3, Palladium, processes ***7440-06-4*** , Platinum, processes 7440-22-4, Silver, processes ***7440-31-5*** , Tin, processes 7440-36-0, Antimony, processes 7440-50-8, Copper, processes ***7440-57-5*** , Gold, processes 7440-66-6, Zinc, processes 7440-69-9, Bismuth, processes 7440-74-6, Indium, processes 9004-34-6, Cellulose, processes 9005-53-2, Lignin, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(structure, materials, and applications of ball grid array interconnections)

National Patent Classification

257778000

International Patent Classification

ICM H01L023-48

☐ L44 ANSWER 4 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number

2000:821610 HCAPLUS Full Text

Title

Direct die contact (DDC) semiconductor package and its fabrication

Author/Inventor

Wood, Alan G.; Farnworth, Warren M.; Grigg, Ford; Akram, Salman

Patent Assignee/Corporate Source

Micron Technology, Inc., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6150717	A	20001121	US 1998-98197	19980616 <--
			US 1997-905602 A	19970804

Abstract

A semiconductor package and method for fabricating the package are provided. The package includes a housing having individual channels, each adapted to retain a semiconductor die in elec. communication with elec. connectors. The dice can include ***solder*** bumps, formed on electrodes, using electroless deposition and wave ***soldering.*** For fabricating the package, the dice can be inserted into the channels, with the elec. connectors on the housing proximate to the ***solder*** bumps on the dice. The ***solder*** bumps can then be reflowed to form bonded connections with the elec. connectors. In an alternate embodiment, conductive adhesive bumps, rather than ***solder*** bumps, are formed on the dice to

provide compliant connections with the elec. connectors on the housing. In addition, the conductive adhesive bumps can be cured while in contact with the elec. connectors to form bonded connections. Other alternate embodiments include a chip scale package, a temporary package for testing bare dice, and a multi chip module.

Concept or Classification

76-3 (Electric Phenomena)

Supplementary Terms

direct die contact semiconductor package packaging

Controlled or Index Terms

Adhesives
(conductive; in direct die contact semiconductor package and fabrication)
Dies
Electronic packages
Electronic packaging process
(direct die contact semiconductor package and fabrication)
Bump contacts
Negative photoresists
Soldering
Solders
(in direct die contact semiconductor package and fabrication)
Metals, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in direct die contact semiconductor package and fabrication)
7429-90-5, Aluminum, processes ***7440-02-0*** , Nickel, processes
7440-05-3, Palladium, processes ***7440-31-5*** , Tin, processes
7440-47-3, Chromium, processes ***7440-57-5*** , Gold, processes
7440-66-6, Zinc, processes 12641-87-1 57923-51-0, Lead 95, tin 5
305799-69-3, Indium 63, tin 37 305799-70-6, Gold 2, lead 62, tin 36
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in direct die contact semiconductor package and fabrication)

National Patent Classification

257738000

International Patent Classification

ICM H01L023-48

☐ L44 ANSWER 7 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number

1999:21646 HCAPLUS Full Text

Title

Method of manufacturing an optical semiconductor device

Author/Inventor

Kurata, Kazuhiko

Patent Assignee/Corporate Source

NEC Corporation, Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5854087	**A**	**19981229**	**US 1996-638873**	**19960429 <--**
JP 07094786	A2	19950407	JP 1994-36171	19940307 <--
JP 2797958	B2	19980917	JP 1993-125114	19930427
US 5917200	A	19990629	US 1995-452653	19950525 <--
			US 1994-233941	19940428

Abstract

Methods of manufacturing an optical semiconductor device, consisting essentially of the steps of: forming a junction portion on an optical circuit substrate, wherein the junction portion comprises: a first Au layer on the optical circuit substrate; a Sn layer on the first Au layer, and a second Au layer having a thickness of 0.4 μm on the Sn layer so that the junction portion has a weight % ratio of Au to Sn of at least 80%:20% after the junction portion is formed; making a junction portion of an optical semiconductor element contact with the junction portion of the optical circuit substrate; pressing the optical semiconductor element to the optical circuit substrate; heating the optical circuit substrate; and cooling the optical circuit substrate. A barrier layer including a Ti layer and, optionally, a Pt layer may be provided on the substrate before the junction portion is formed.

Concept or Classification

73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76

Supplementary Terms

optical semiconductor device ***gold tin solder***

Controlled or Index Terms

Solders
(optical semiconductor device manufacture using melted gold and tin layers for)
Electric contacts
Semiconductor device fabrication
(optical semiconductor device manufacture using melting of gold and tin layers for junction formation)
Semiconductor devices
(optical; optical semiconductor device manufacture using melting of gold and tin layers for junction formation)
Optical instruments
(semiconductor; optical semiconductor device manufacture using melting of gold and tin layers for junction formation)
7440-06-4 , Platinum, uses 7440-32-6, Titanium, uses
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(barrier layer; optical semiconductor device manufacture using melting of gold and tin layers for junction formation)
12727-40-1, Gold 80, tin 20
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(optical semiconductor device manufacture using melting of gold and tin layers for junction formation)
7440-31-5 , Tin, uses ***7440-57-5*** , Gold, uses
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(optical semiconductor device manufacture using melting of gold and tin layers for junction formation)
7440-21-3, Silicon, uses
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(substrate; optical semiconductor device manufacture using melting of gold and tin layers for junction formation)

National Patent Classification

438026000

International Patent Classification

ICM H01L021-283
ICS H01L021-58

☐ L44 ANSWER 9 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
1998:41936 HCAPLUS Full Text

Title
Multilayer Au -Sn solder for photosemiconductor substrates

Author/Inventor
Hirai, Ayumi; Kaku, Yoshiji

Patent Assignee/Corporate Source
Japan Aviation Electronics Industry Ltd., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10006073	**A2**	**19980113**	**JP 1996-152683**	**19960613 <--**
JP 3303227	B2	20020715	JP 1996-152683	19960613

Abstract
A ***solder*** consisting of alternate Au and Sn layers is formed on a photosemiconductor element substrate with the upper layer being a Au layer. The layers of each type have approx. the same thickness and form an eutectic ***solder*** mixture containing 80 weight% Au. The Sn layers have a thickness of ≤3000 Å (calculated as bulk d.). A bonding layer consisting of Ti, Cr, or Pt may be provided between the Au layer and substrate. The bonding layer may also have a ***multilayer*** structure. Oxidation prior to alloying of the ***solder*** , that occurs when the ***multilayer solder*** is melted, is prevented.

Concept or Classification
56-9 (Nonferrous Metals and Alloys) Section cross-reference(s): 76

Supplementary Terms
photoconductor ***gold tin multilayer solder***

Controlled or Index Terms
Photoconductors
Solders
(***multilayer Au -Sn solder*** for photosemiconductor substrates)
12727-40-1, Gold 80, tin 20
RL: DEV (Device component use); USES (Uses)
(average composition; ***multilayer Au -Sn solder*** for photosemiconductor substrates)
7440-02-0 , Nickel, uses 7440-05-3, Palladium, uses ***7440-06-4*** , Platinum, uses 7440-32-6, Titanium, uses 7440-47-3, Chromium, uses
RL: DEV (Device component use); USES (Uses)
(bonding layer containing; ***multilayer Au -Sn solder*** for photosemiconductor substrates)
7440-31-5 , Tin, uses ***7440-57-5*** , Gold, uses
RL: DEV (Device component use); USES (Uses)
(***multilayer Au -Sn solder*** for photosemiconductor substrates)

International Patent Classification
ICM B23K035-14
ICS B23K035-30; H01L021-52; H01S003-18; H05K003-24; H05K003-34

☐ **L44 ANSWER 11 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number
1997:757002 HCAPLUS Full Text

Title
***Solder* pastes with an alloy and eutectic components for reflow bonding of integrated circuits**

Author/Inventor
Paruchuri, Mohan R.; Shangguan, Donkai; Achari, Achyuta

Patent Assignee/Corporate Source
Ford Motor Company, USA; Ford Motor Company Limited; Ford Motor Company of Canada Limited

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
(1) WO 9743081	**A1**	**19971120**	**WO 1997-GB1186**	**19970501 <--**
			US 1996-644765 A	**19960510**
CA 2253483	AA	19971120	CA 1997-2253483	19970501 <--
(2) EP 946330	A1	19991006	EP 1997-918275	19970501 <--
JP 2000511466	T2	20000905	JP 1997-540613	19970501 <--
EP 1084790	A1	20010321	EP 2000-122960	19970501 <--

Abstract
The ***solder*** pastes suitable for reflow ***soldering*** of electronic parts at high d. to printed-circuit boards at decreased temperature contain: (a) powder of ***binary***, ternary, or eutectic alloys of Sn-Bi-In type with the m.p. below the heat-deflection temperature of the laminated boards; (b) Sn or Sn-alloy powder reacting with the 1st powder in ≤15 min at 150°, and having the m.p. above the heat-deflection temperature; (c) minor alloying addns. of Cu, Ni, Ag, Ce, In, Bi, and/or Au added to enhance the wetting and reflow properties; and (d) temporary carrier, binder, and flux for paste mixts. The powder mixture for reflow melting at 120° contains ternary Bi-24.8 In-18.0% Sn eutectic with the m.p. of 77.5°, and Sn (m.p. 232°) at nominally 1:1 weight ratio, and shows the post-reflow m.p. increased by the alloying reaction to 160-180° for harder ***solder*** residue and stronger joints. The ***solder*** mixture is suitable for use with the elec.-circuit boards made of thermoplastic polymers with the heat-deflection temperature of 100-150°.

Concept or Classification
56-9 (Nonferrous Metals and Alloys) Section cross-reference(s): 76

Supplementary Terms
solder paste alloy powder eutectic mixt; elec circuit ***soldering*** eutectic alloy paste; thermoplastic elec board ***soldering*** alloy paste; bismuth alloy ***solder*** paste reflow temp; tin alloy ***solder*** paste reflow temp

Controlled or Index Terms
Solders
Solders
(paste, alloy mixture for; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
Soldering
(reflow, paste for low-temperature; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
Pastes
Pastes
(***solder***, alloy mixture for; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits

on thermoplastic boards)
Printed circuit boards
(***soldering*** of; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
Plastics, uses
RL: DEV (Device component use); USES (Uses)
(thermoplastics, elec. circuit boards, ***solders*** for; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
12673-36-8 65187-66-8 79484-04-1 143497-52-3 150922-03-5 158822-74-3 164466-60-8 199856-49-0 199856-50-3
RL: MOA (Modifier or additive use); USES (Uses)
(eutectic, ***solder*** mixts. containing; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
7440-31-5 , Tin, uses 80954-92-3
RL: MOA (Modifier or additive use); USES (Uses)
(powder, ***solder*** mixture with; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
50951-31-0 199856-47-8
RL: MOA (Modifier or additive use); USES (Uses)
(***solder*** mixts. containing; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
7440-50-8, Copper, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(***soldering*** to, on elec.-circuit boards; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)
7440-02-0 , Nickel, uses 7440-22-4, Silver, uses 7440-45-1, Cerium, uses ***7440-57-5*** , Gold, uses 7440-69-9, Bismuth, uses 7440-74-6, Indium, uses
RL: MOA (Modifier or additive use); USES (Uses)
(***solders*** containing; ***solder*** pastes with alloy and eutectic powder mixts. for reflow bonding of elec. printed circuits on thermoplastic boards)

International Patent Classification
ICM B23K035-26
ICS B23K035-14; H05K003-34

☐ L44 ANSWER 14 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
1996:506141 HCAPLUS Full Text

Title
Solder and its use for making a soldered joint between two objects

Author/Inventor
Huebner, Holger

Patent Assignee/Corporate Source
Siemens A.-G., Germany

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
(1) WO 9619314	**A1**	**19960627**	**WO 1995-DE1742**	**19951205 <--**
			DE 1994-4446068	19941222

Abstract

A ***solder*** consists of a 1st metal component, a 2nd metal component, and a filler, in which the 1st metal component has a higher m.p. than the 2nd component and in which the 1st metal component and the molten 2nd metal component form an ***intermetallic*** phase having a m.p. above the working temperature at the temperature which is below the m.p. of the 1st component. The filler is wetted by the molten 2nd metallic component and is substantially insol. at the working temperature The ***solder*** is suitable for making joints between 2 objects. At a working temperature in the region of the m.p. of the 2nd metallic component, the ***soldered*** joint is formed by isothermal solidification as a matrix from the ***intermetallic*** phase, in which the filler forms an inner surface.

Concept or Classification

56-9 (Nonferrous Metals and Alloys)

Supplementary Terms

solder alloy

Controlled or Index Terms

Solders
(alloys for improved)
Ceramic materials and wares
(in ***solder***)
Glass, oxide
RL: NUU (Other use, unclassified); USES (Uses)
(in ***solder***)
Polymers, uses
RL: NUU (Other use, unclassified); USES (Uses)
(metalized; in ***solder***)
7429-90-5, Aluminum, uses ***7439-89-6*** , Iron, uses 7439-92-1, Lead, uses 7439-96-5, Manganese, uses 7439-97-6, Mercury, uses ***7440-02-0*** , Nickel, uses 7440-05-3, Palladium, uses 7440-21-3, Silicon, uses 7440-22-4, Silver, uses ***7440-31-5*** , Tin, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-36-0, Antimony, uses 7440-47-3, Chromium, uses ***7440-48-4*** , Cobalt, uses 7440-50-8, Copper, uses 7440-55-3, Gallium, uses ***7440-57-5*** , Gold, uses 7440-62-2, Vanadium, uses 7440-66-6, Zinc, uses 7440-69-9, Bismuth, uses 7440-74-6, Indium, uses
RL: NUU (Other use, unclassified); USES (Uses)
(in ***solder***)

International Patent Classification

ICM B23K035-26
ICS B23K035-02; B23K035-30

☐ L44 ANSWER 18 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number

1996:30114 HCAPLUS Full Text

Title

Soldered or brazed joints including stress-release layers and barrier interlayers for increased reliability

Author/Inventor

Chan, Chin Jong; Chang, Jei Wei; Romankiw, Lubomyr T.

Patent Assignee/Corporate Source

International Business Machines Corp., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5471092	A	19951128	US 1994-360528	19941221 <--
			US 1992-945309	19920915

Abstract

The ***multilayered*** joint in ***soldering*** or ***brazing*** includes: (a) an adhesion-promoting surface layer on the 1st joint component; (b) soft metal interlayer for stress release; (c) hard barrier interlayer resistant to Sn, and selected from Cr, Ti-W, and/or Ta; (d) phased-metal interlayer; (e) ***solder*** -reactive metal interlayer typically selected from Cu, Ni, Co, Au, Ag, Pt, Pd, Rh, Ni-P, and/or Co-P alloys; and (f) ***solder*** or ***braze*** layer selected from Pb-***Sn*** , ***Au*** -***Sn*** , Pb-In, Au-In, Au-In-Sn, and Bi-Sn alloys, and positioned next to the 2nd joint component. The process is suitable for joining of elec.-circuit chips to semiconductor or ceramic substrates with improved reliability by decreased internal stress. The optimized ***soldering*** joint on metalized glass substrate was obtained by the ***multilayer*** assembly with Cr film (200 Å thick) adhesion layer, Au film (700 Å) as soft interlayer, Cr film (300 Å) as hard barrier interlayer, and Cu and Sn at 3 films each controlled to form Cu3Sn layer in ***brazing***.

Concept or Classification

56-9 (Nonferrous Metals and Alloys) Section cross-reference(s): 76

Supplementary Terms

elec circuit ***soldering*** ***multilayer*** joint; ***soldering*** ***multilayer*** joint stress release; ***brazing*** ***multilayer*** joint stress release; glass metalizing ***multilayer*** stress release; copper tin ***braze*** joint diffusion alloying

Controlled or Index Terms

Glass, oxide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(metalized, ***brazing*** or ***soldering*** of; joints including stress-release layers and barrier interlayers in diffusion alloying)

Soldering
(***multilayer*** ; joints including stress-release layers and barrier interlayers for increased reliability)

Soldering
(***brazing*** , ***multilayer*** ; joints including stress-release layers and barrier interlayers in diffusion alloying)

Electric circuits
(integrated, ***brazing*** or ***soldering*** of; joints including stress-release layers and barrier interlayers in diffusion alloying)

12785-33-0 173046-82-7
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(***braze*** interlayer; ***soldering*** joints including stress-release layers and barrier interlayers in diffusion alloying)

12019-61-3
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(interlayer; ***brazing*** joints including stress-release layers and barrier interlayers in diffusion alloying)

7440-02-0 , Nickel, processes 7440-05-3, Palladium, processes
7440-06-4 , Platinum, processes 7440-16-6, Rhodium, processes
7440-22-4, Silver, processes 7440-25-7, Tantalum, processes
7440-31-5 , Tin, processes 7440-32-6, Titanium, processes
7440-47-3, Chromium, processes ***7440-48-4*** , Cobalt, processes
7440-50-8, Copper, processes ***7440-57-5*** , Gold, processes
11146-55-7 12711-58-9
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(interlayer; ***brazing*** or ***soldering*** joints including stress-release layers and barrier interlayers in diffusion alloying)

11110-54-6 11110-87-5 12713-30-3 37334-21-7
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(***solder*** interlayer; ***soldering*** joints including
stress-release layers and barrier interlayers in diffusion alloying)

National Patent Classification
257753000

International Patent Classification
ICM H01L023-48
ICS H01L029-46

☐ L44 ANSWER 23 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
1994:151628 HCAPLUS Full Text

Title
Circuit boards with metal films for forming soldered contacts, their fabrication, and electronic switch assemblies using the boards and their fabrication

Author/Inventor
Harada, Masahide; Ando, Akihiro; Satoh, Ryohei; Yabushita, Akira; Kanda, Naoya; Horikoshi, Kazuhiko

Patent Assignee/Corporate Source
Hitachi, Ltd., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 4301728	A1	19930729	DE 1993-4301728	19930122 <--
DE 4301728	C2	19971211	JP 1992-9299 A	19920122
US 5476726	**A**	**19951219**	**US 1993-5353**	**19930119 <--**
JP 06077286	A2	19940318	JP 1993-7385	19930120
JP 3172308	B2	20010604	JP 1992-9299 A	19920122
			JP 1992-164545 A	19920623

Abstract
The title circuit boards are provided with a metal film comprising a mixture of a 1st metal that can easily be wetted by the metals forming the ***solder*** and that readily forms an alloy or ***intermetallic*** compound and a 2nd metal that is not easily wetted with the ***solder*** and that does not melt (e.g., during ***soldering***). Methods for producing the boards include the formation of metal films like those described above. Electronic switching assemblies are also described for which the switch components are mounted on the above described circuit boards; their fabrication includes ***soldering*** contacts to the metal film.

Concept or Classification
76-14 (Electric Phenomena)

Supplementary Terms
circuit board contact layer metal mixt; electronic switch circuit board contact layer

Controlled or Index Terms
Electric switches and switching
(assemblies, mounted on circuit boards with ***multilayer*** contact structures)
Electric contacts
(***multilayer*** structures, ***solderable***)
Electric circuits
(printed, boards, ***multilayer*** contact structures for)
7440-02-0 , Nickel, uses ***7440-06-4*** , Platinum, uses

7440-31-5 , Tin, uses 7440-50-8, Copper, uses ***7440-57-5***
, Gold, uses 11105-41-2 11110-54-6 11110-87-5 11124-13-3
11144-61-9 11149-13-6 12668-71-2 12683-71-5 12713-30-3
12785-33-0 12798-70-8 37263-08-4 39303-75-8 39460-91-8
56925-19-0 66758-10-9 80954-92-3 82151-12-0 153271-61-5, Antimony,
gold , ***tin***
RL: USES (Uses)
(elec. circuit board contact layers containing)

International Patent Classification
ICM H05K001-09
ICS H05K003-16; H05K003-34; B23K035-24

☐ L44 ANSWER 32 OF 32 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
1974:483576 HCAPLUS Full Text

Title
Semiconductor structure with bumps

Author/Inventor
Rose, Ralph Edward

Patent Assignee/Corporate Source
Signetics Corp.

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 3821785	**A**	**19740628**	**US 1972-238116**	**19720327 <--**
CA 984060	A1	19760217	CA 1973-165113	19730302 <--
GB 1377601	A	19741218	GB 1973-10881	19730306 <--
DE 2314731	A1	19731011	DE 1973-2314731	19730324 <--
FR 2178007	A1	19731109	FR 1973-10813	19730326 <--
JP 49009187	A2	19740126	JP 1973-34978	19730327 <--
JP 52000670	B4	19770110	US 1972-238116	19720327
IT 981659	A	19741010	IT 1973-22206	19730327 <--
US 3874072	**A**	**19750401**	**US 1973-392112**	**19730827 <--**
			US 1972-238116	19720327

Abstract
A semiconductor structure is provided with bumps or pillars which can withstand thermal cycling without breaking or shearing. Metallic contact pads are formed over a planar semiconductor surface and a layer of insulating material is formed over the contact pads. Bumps or pillars consisting of relatively ductile thick Al layers are formed to extend through the insulating material and are bonded to the contact pads. A mushroom-shaped base region (e.g. of Ni) is secured to the ductile layer over a Cr diffusion-barrier layer. ***Au*** -***Sn*** layers are used to bond the bumps or pillars to the lead frames. The base region keeps the lead which is ***soldered*** to the top of the bump from being pressed down to the pad and shorting on the edge of the chip. The structure accommodates 2-3 μ of movement without damage.

Concept or Classification
71-13 (Electric Phenomena)

Supplementary Terms
semiconductor contact structure; aluminum contact semiconductor; nickel contact semiconductor; chromium contact semiconductor

Controlled or Index Terms

Electric contacts
(bumps, for semiconductor devices, stable against thermal cycling)
Semiconductor devices
(contact bumps for, stable agaainst thermal cycling)
7429-90-5, uses and miscellaneous ***7440-02-0*** , uses and miscellaneous 7440-47-3, uses and miscellaneous
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(elec. contact bumps, stable against thermal cycling, for semiconductor devices)
7440-31-5 , uses and miscellaneous ***7440-57-5*** , uses and miscellaneous
RL: USES (Uses)
(***solders*** , for contact bumps to lead frames in semiconductor circuits)

National Patent Classification
357067000

International Patent Classification
H01L

L54 ANSWER 6 OF 31 PCTFULL COPYRIGHT 2004 Univentio on STN

Accession Number

1998039781 PCTFULL ED 20020514 Full Text

Title

VERTICALLY INTERCONNECTED ELECTRONIC ASSEMBLIES AND COMPOSITIONS USEFUL THEREFOR
ENSEMBLES ELECTRONIQUES INTERCONNECTES VERTICALEMENT ET COMPOSITIONS UTILES AFFERENTES

Author/Inventor

GALLAGHER, Catherine, A.; MATIJASEVIC, Goran, S.; GANDHI, Pradeep; CAPOTE, M., Albert

Patent Assignee/Corporate Source

ORMET CORPORATION

Patent Information

WO 9839781	A1 19980911 <-----------

Priority Application Information

US 1997-8/813,809	19970306

Abstract

In accordance with the present invention, ***multilayer*** printed circuit boards are provided, the structure of which comprises a plurality of layers (a)-(c) as follows, so as to achieve the desired multiplicity of layers: (a) a bottom circuit layer; (b) a via interconnect layer; and (c) a top circuit layer. In another aspect, the present invention is directed to a ***multilayer*** printed circuit board with an attached component or die, the structure of which comprises: (a) a single or ***multilayer*** printed circuit board substrate; (b) a via interconnect layer which has electrically conductive adhesive compositions patterned into suitable dielectric materials, where the suitable dielectric materials provide adhesion between the printed circuit board and a component or die while the electrically conductive adhesive compositions provide the electrical interconnection and
adhesion between connecting pads of the printed circuit board substrate and the attached component or die; and (c) an area array component package or bare die which is attached to the printed circuit board layer with the use of said suitable patterned dielectric materials.

Description

5,376,403, the entire contents of which are hereby incorporated by reference herein. The electrically conductive adhesive compositions contemplated for use herein comprise a ***solder*** powder, a latent or chemically protected crosslinking agent with fluxing properties and a reactive monomer or polymer. Depending upon the intended end use, compositions contemplated for use herein comprise three or more of the following.

relatively high melting metal powder (hereinafter, metal powder); lower melting point metal powder (hereinafter, ***solder*** powder) ; crosslinking agent which also serves as a fluxing agent; binder; and reactive monomer or polymer.

(1) A low melting point' metal or metal alloy powder (***solder***); (2) A crosslinking agent comprising a latent or protected curing agent, which also acts as a primary fluxing agent; (3) Optionally, a high melting point metal or metal alloy powder; (4) Optionally, a binder; (5) Optionally, a reactive monomer or polymer which can be crosslinked by the curing agent (hereinafter referred to as the monomer), and (6) Optionally, a metal additive.

The compositions employed in the practice of the present invention frequently also contain at least one solvent; they may also contain other additives to improve certain properties such as adhesion, rheology or

solderability.

The low melting point metal or metal alloy powder (1) contemplated for use herein may be Sn, Bi, Pb, Cd. Zn, Ga, In, Te, Hg, Tl, Sb, Se, Po, or the like, as well as an alloy or other metal having a melting point lower than that of the metal powder in (3). Typically, the powder has a mean particle diameter of 1-40 microns; preferably, the average particle diameter is less than or equal to the average diameter of the high melting point metal particles and the particle size distribution is substantially the same as that of the high melting point metal powder (when present) . The principal requirement of the *solder* alloy is that it flow in the composition before the vitrification of the polymers in the composition. In order f or this to occur, the *solder* alloy must readily wet the high melting point metal (3) For this reason, alloys of tin are ideal.

Protection may also be achieved mechanically, for example, by encapsulating the curing agent in a shell of non- reactive material which releases the curing agent only at or near the melting time of the *solder* powder.

is (a) A bulk electrical conductivity approaching that of solid copper (never achieved with prior art compositions); (b) good *solderability* of the cured compositions; (c) adhesive strengths comparable to copper-clad epoxy printed wiring board laminates; (d) highly corrosion resistant f inal products with resistance to degradation at high temperatures and high relative humidities; (e) *low process temperatures* compatible with polymer printed wiring board substrates; and (f) fabrication processes with significantly fewer process steps than conventional PWB fabrication methods.

The electrical conductivity of the compositions employed in the practice of the invention is superior to the performance of conductive polymer thick films which generally incorporate high levels of silver or copper particles into a thermosetting or thermoplastic resin binder and rely upon mechanical contact of these particles to carry electrical current. In contrast to the metal content employed in PTF compositions, inventive compositions employ a combination of a high melting point metal and a relatively low melting point alloy which undergo a process known as transient-liquid-phase sintering (TLPS) to form true metallurgical joints between the metal particles, Sintering is a well known technique used to fabricate wiring in *multilayer* substrates in ceramic technology. In this technique, however, process temperatures in excess of 7000C are used to eliminate the organic binder and reduce the metal oxides for complete densification. In contrast, several metallurgical systems can undergo TLPS at temperatures well below 3500C. TLPS is characterized by raising a low melting point metal or alloy to its melting temperature at which time it diffuses into a higher melting point metal or alloy. The new alloy thus formed solidifies as it is created and has an entirely new melting point. Judicious choice of metals employed in the TLPS process can provide a composition that will *remelt* at substantially higher temperatures than the melting point of the original low melting point alloy. This property can readily be exploited in the practice of the present invention, thus allowing inventive compositions to be utilized in multiple sequentially processed layers and in standard *soldering* operations without the *remelting* of the originally formed metal matrix in the composition.